(12) UK Patent Application (19) GB (11) 2 222 306 (13) A

(43) Date of A publication 28.02.1990

(21) Application No 8819949.2

(22) Date of filing 23.08.1988

(51) INT CL⁴
H01L 29/78 49/02

(52) UK CL (Edition J)
H1K KCAA KCAL K1CA K4C11 K4C14 K4C2A K4H1A K4H3A K9B1 K9D1 K9E K9N3 K9R2

(56) Documents cited
EP 0175215 A EP 0166261 A2 US 3673471 A

(58) Field of search
UK CL (Edition J) H1K KCAA KCAL KCAX
INT CL⁴ H01L

(71) Applicant
The Plessey Company plc

(Incorporated in the United Kingdom)

Vicarage Lane, Ilford, Essex, IG1 4AQ, United Kingdom

(72) Inventor
John Nigel Ellis

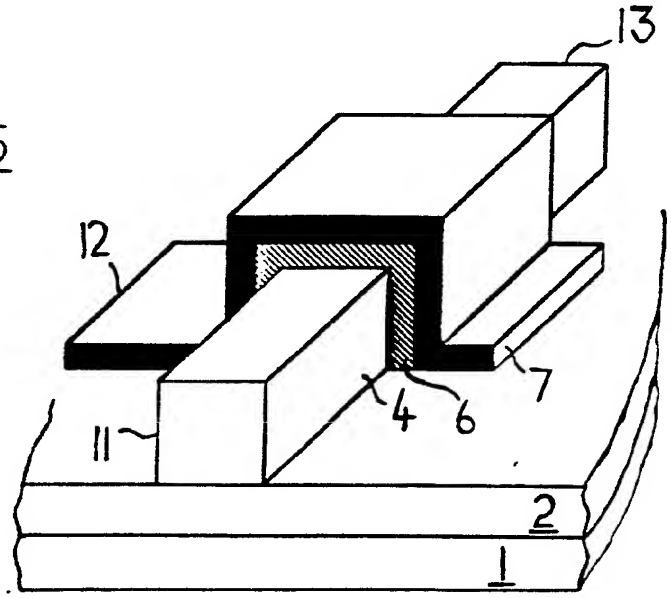
(74) Agent and/or Address for Service
E Pritchard
The Plessey Company plc, Intellectual Property Department, Vicarage Lane, Ilford, Essex, IG1 4AQ, United Kingdom

(54) **Field effect transistor**

(57) A MOSFET comprises a body 1 of semiconductor wafer material supporting an electrical insulation layer 2, the layer carrying a semiconductor island 4 covered by a dielectric film 6 which in turn supports a first electrode area 7 constituting a gate or control electrode, the island 4 comprising source and drain electrode areas. The material of the gate electrode together with the values for depletion width and doping level in the semiconductor island are selected so that operation in a volume inversion or volume enhancement mode can be obtained when suitable potentials are applied to the electrode areas.

This can give a Volume Inversion or Volume Enhancement MOSFET having an enlarged volume with in which inversion can take place.

Fig. 5



GB 2 222 306 A

2222306

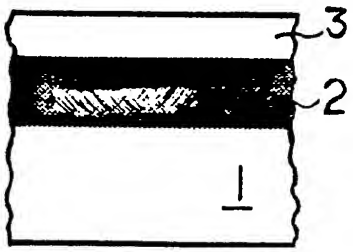


Fig.1

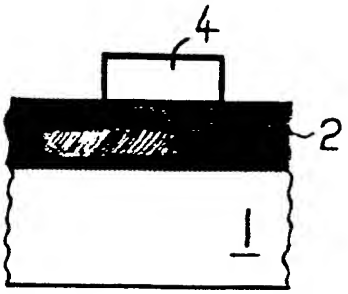


Fig.2

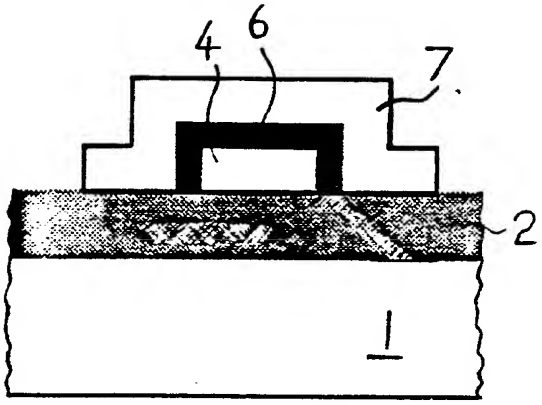


Fig.3

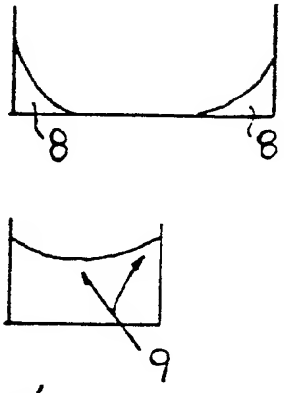


Fig.4

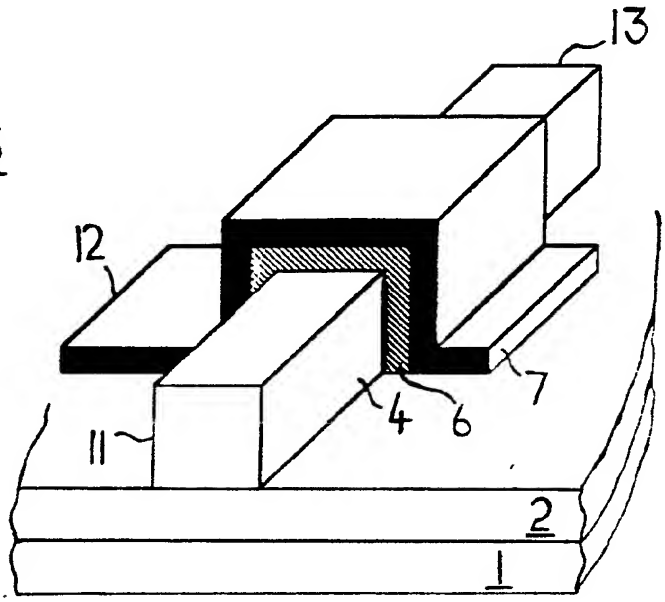


Fig.5

2222306

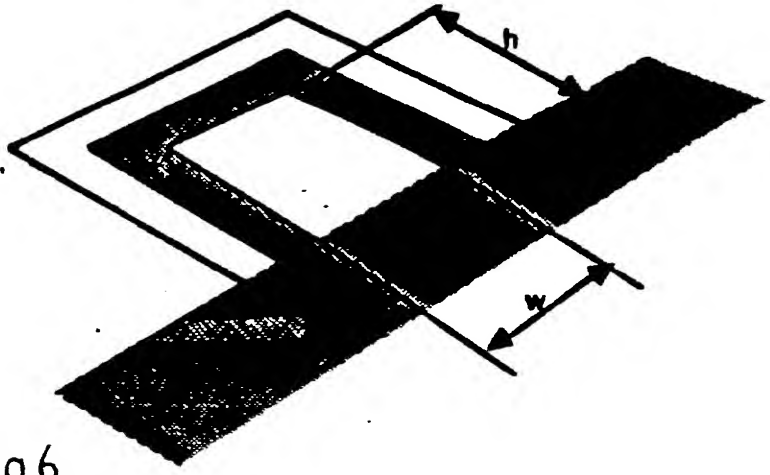


Fig.6

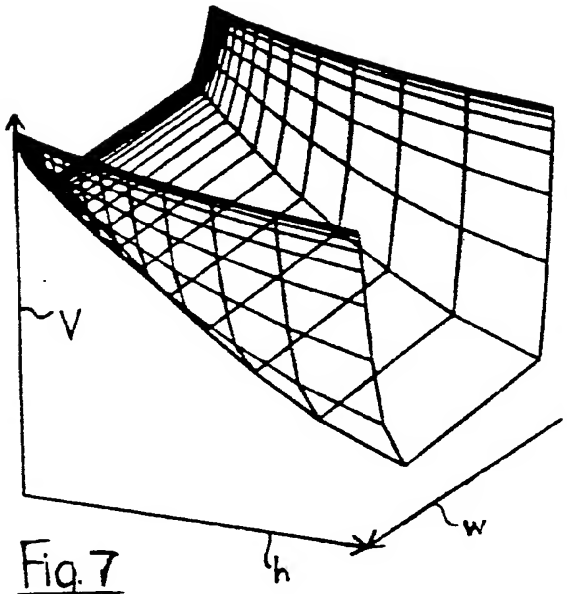


Fig.7

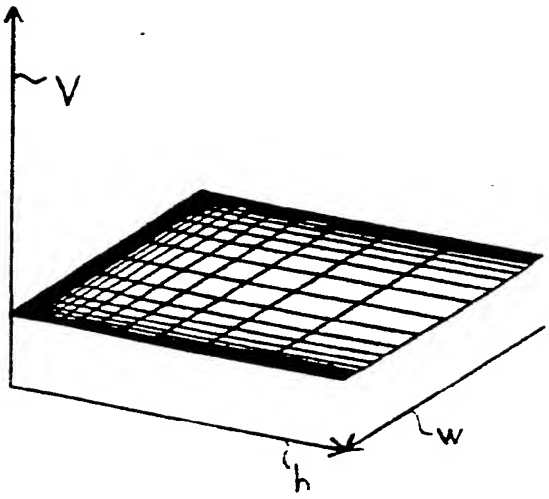


Fig.8

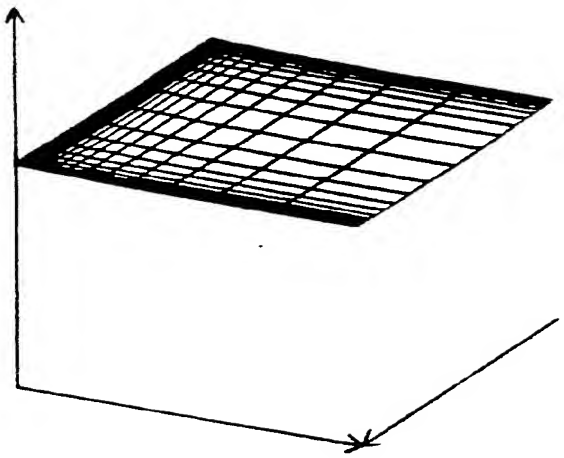


Fig.9

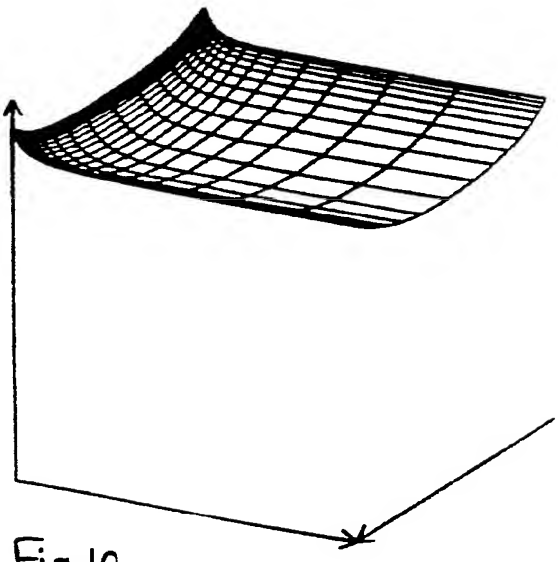


Fig.10

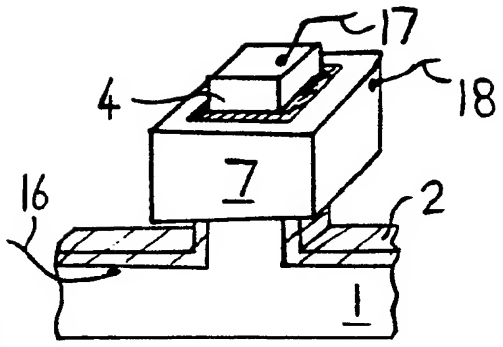


Fig.11

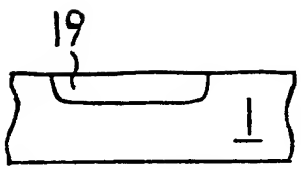
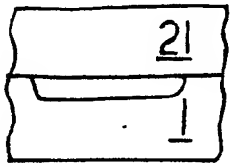
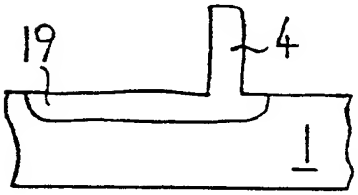


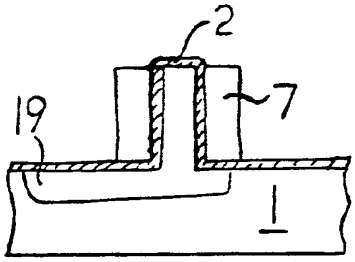
Fig. 12 A



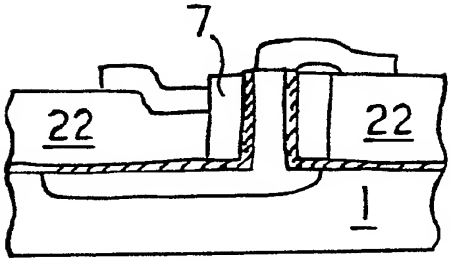
B



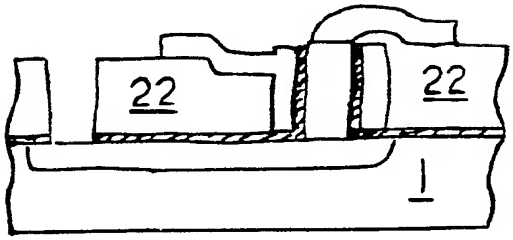
C



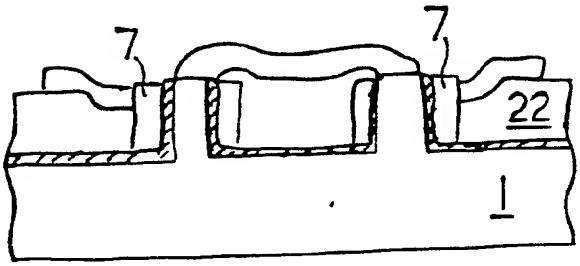
D



E



F



G

SEMICONDUCTOR DEVICES

This invention relates to semiconductor devices. It relates particularly to a semiconductor device of the metal oxide semiconductor field effect transistor (MOSFET) type and to a method of manufacture of such a device.

A volume inversion MOSFET (or VIMOSFET) type of device has been described by Christoloveanu et al in Properties of Front and Buried Interfaces of Oxygen Implanted SOI Films Deduced from MOS Device Characteristics, Insulating Films on Semiconductors, J.J. Simonne and J. Buxo (Editors), Elsevier Science (North Holland) 1986, pages 49 to 52, and in Electrical Properties of Simox Materials and Devices, Physics and Technology of Amorphous Silica, Les Arcs, France, July 1987. This device operates by making use of two gate electrodes which are located on opposite sides of a silicon substrate and which are closely spaced from one another. This construction results in the formation of a silicon filament region which is sufficiently narrow in width so as to permit a volume inversion effect to occur. It has been reported by several authors that this behaviour can increase the potential drive power of the device as compared with that of a conventional MOSFET by allowing the whole volume of a region of silicon to invert in addition to an inversion which occurs at the conventional surfaces.

The VIMOSFET construction described in the aforementioned publications relies on implanting two oxygen films in the silicon substrate in order to generate a vertical filament region. This is usually a costly and difficult technique to put into practise.

The present invention relates to an alternative device construction which can avoid any difficulties which might occur with the need for etching narrow trenches or implanting multiple oxide layers.

According to the invention, there is provided a semiconductor device, comprising a body of semiconductor wafer material supporting an electrical insulation layer, the layer carrying a semiconductor island covered by a dielectric film which in turn supports a first electrode area constituting a gate or control electrode, the island forming source and drain electrode areas, the construction further including a conductive region adjoining each electrode area to support external electrical connections for the device, the material of said gate electrode together with the values for depletion width and doping level in the semiconductor island being selected such that operation in a volume inversion or volume enhancement mode can be obtained when suitable potentials are applied to said electrode areas.

In one form of construction, the island has a rectilinear shape with two distinct side portions which define interfaces from which semiconductor depletion regions can develop and grow. The said side portions are separated by an area of the island which is so dimensioned as to enable said depletion regions to coalesce whereby volume inversion of a useful part of the island area can occur.

In one embodiment, the two island side portions are accompanied by a third side portion capable of forming its own depletion region. The coalescence of the said three depletion regions

can enable a greater proportion of the island area to exhibit the volume inversion effect.

The invention further comprises a method of construction of a semiconductor device, the method comprising the steps of providing a body of semiconductor wafer material, creating an electrical insulation layer on said wafer, forming a narrow semiconductor island on said layer, doping said island to form a transistor body, forming a dielectric film on said body, depositing a gate electrode area on said film, forming source and drain electrode areas, laying down an interlayer dielectric material, making contact openings then depositing metal regions to provide external electrical connections for the resulting device, the material of said gate electrode together with the values for depletion width and doping level in the semiconductor island being selected such that operation in a volume inversion or volume enhancement mode can be obtained when suitable potentials are applied to said electrode areas.

The insulation layer may be formed by a process such as an oxygen implantation, porous anodisation, recrystallisation, growth of silicon on sapphire (SOS) or vapour deposition process.

The said semiconductor island may be formed by a photolithography and anisotropic plasma etching process.

Preferably, the interlayer dielectric material is formed by a phosphorosilica glass (PSG) or other glass deposit.

By way of example, a particular embodiment of the invention will now be described with reference to the accompanying drawings, in which:

Figure 1 is a cross-sectional view of the device starting material,

Figure 2 shows the etched semiconductor island,

Figure 3 shows the main parts of the completed device,

Figure 4 shows the inversion areas that can be present with wide and narrowly-spaced gate electrode regions,

Figure 5 is a perspective view of the complete device,

Figures 6 to 10 show various simulation diagrams to explain operation of the device of the invention,

Figure 11 shows a further construction of the device having four sides, and,

Figures 12A to G show different stages in the construction of the four-sided device.

As depicted in Figure 1, construction of the device of the invention begins with preparation of a substrate body 1 which in this example is an area of a silicon semiconductor wafer material. A layer of electrical insulation material 2 is formed on this substrate by a process of porous anodisation, or in a different embodiment this might be effected by oxygen implantation.

A film 3 of semiconductor material is then formed on top of the insulation layer, this film is next covered with a photoresist material which is subsequently exposed to light through a mask and developed. The result of these operations is to provide a masking material cover over separate areas of the film in order to protect these areas for carrying out an etching operation. The assembly is then treated in a reactive ion etching process which serves to remove portions of the film in areas which are not protected by the masking

material. The remaining traces of masking material are then removed, and the insulation layer will be seen now to support a separate, well-defined island 4 (Figure 2) of the semiconductor material.

The island 4 is then doped to form a CMOS transistor area of a predetermined conductivity type.

A body 6 (Figure 3) of gate oxide is then grown around the transistor area using a technique which gives reliable corner oxide integrity. Next, a gate electrode conductor material 7 such as polysilicon is deposited on the oxide surface and printed and etched in a conventional manner.

The assembly then has source and drain electrode regions implanted therein by using a mask such as the kind used for fabricating n- or p- type transistor devices. This step is followed by a phosphorosilica glass (PSG) or other glass interlayer dielectric deposition, and the deposit is then subjected to flow and activation as in a conventional process.

Finally, contacts are etched and metal is deposited and defined as in the construction of a conventional semiconductor device.

In operation of this device, when suitably connected to a power supply, as the gate electrode voltage is raised from a low voltage (zero or minus one or two volts) to a higher voltage (plus one or two volts) the semiconductor first depletes as in an ordinary MOSFET device. The depletion regions are then required to meet and sweep out the whole of the enclosed area of silicon. When this state is present, the potential of the inner part of the silicon, which is

normally a depleted part, can be raised sufficiently to invert the whole volume.

A device having a silicon on insulator construction is suitable for the VIMOSFET formation as it allows fabrication by means of simple but fine-line patterning techniques. This can eliminate difficulties which may occur with etching trenches, or implanting multiple oxide layers by conventional techniques.

Figure 4 shows the result of the volume inversion effect in the transistor body both when the gate electrode regions are widely spaced and when they are closely spaced. The widely spaced gate electrode regions allow a small volume 8 of the inverted area to appear at each side but when they are closely spaced the regions join together to cause an enlarged volume 9 of the inversion area to appear. This available additional area for conduction as compared with that of the conventional MOSFET device depends partly on the values for doping density and distance, since a lighter doping level will allow a larger size of island to be employed. Typically the geometry will be 0.5 micrometres and doping levels of 1E15 - 1E16 will be used.

The range of geometry over which this device is able to operate is dependent on the doping level. It can be determined approximately by the expression

$$w = (2eV/qn)^{1/2}$$

where e = permittivity of channel material

q = proton charge

n = doping level

which relates the value w for the classical depletion width to the potential V; the magnitude of the potential being chosen to represent the maximum variation desired.

This means that at low doping levels, of around ten to the power of fourteen, a geometry of the dimensions of one micron or more could exhibit this effect, at 0.5 microns the doping level could be higher to around ten to the fifteen and at 0.1 microns, it could be ten to the sixteen per cubic centimetre.

The required relationship between doping and distance is such as to allow the separated depletion regions to meet and join together before the inversion process occurs. The potential may be increased or reduced to permit volume inversion or enhancement to occur depending on the doping levels and electrode material.

The device construction further allows for the transistor to operate in either a volume inversion or a volume enhancement mode the selection of which mode depending only on the doping polarity of the channel in relation to the terminal electrode regions and the work function or doping level of the material used for the gate or control electrode.

Figure 5 is a perspective view of a practical construction of the complete semiconductor device. As seen in this Figure, the substrate body 1 supports the electrical insulation material 2 and this in turn carries the semiconductor island 4. The island 4 is surrounded by the gate oxide body 6 and this is covered by gate electrode conductor material 7.

The electrode areas of the device are provided by the semiconductor island 4 and the end of this body which extends

towards the front of the Figure forms a source electrode terminal 11. The gate electrode conductor material 7 forms a gate electrode terminal 12. An end of the semiconductor island 4 which extends towards the rear of the Figure forms a drain electrode terminal 13. Connection leads (not shown) may thus be secured to the electrode terminals 11, 12 and 13 to enable the device to be tested and put into use.

The operation of the device will now be described in greater detail with reference to the simulation diagrams given in Figures 6 to 10.

When suitably connected to a power supply, the structure may operate as either a volume inversion or an enhancement device depending on the channel polarity, channel doping and gate material used. For the purposes of illustration, an n-channel inversion mode device will first be described and then the difference for operation in the enhancement mode will be given.

Figure 6 shows the device as oriented for simulations in the description which follows. The references "h" and "w" refer respectively to the height and width of the semiconductor island region. The graphs which follow show the Potential Distribution (V) at a standard value for height, where h=0.5 micron, but for different values of width and bias voltage. Potential Distribution is thus shown on a vertical axis and height (h) and width (w) on two horizontal axes as indicated.

Figure 7 shows the potential for a transistor of this type with large dimensions. The device has a width of five microns and an applied bias of 0.1 volt. The potential can be seen to fall from the

interfaces to the centre as would be expected for a conventional transistor device.

Figure 8 shows the potential for a small device of 0.1 micron in width and with the applied bias of 0.1 volt. It can be seen that the potential distribution is virtually flat, thus illustrating the presence of the volume inversion effect.

In an n-channel version of this device, the gate electrode material could be n-doped polysilicon, the channel p-type silicon and the terminals n-type silicon. As the gate electrode voltage is raised from a small negative value to a small positive value, limits typically being five volts but these are not necessarily restricted to this value, the channel region is first enhanced meaning that it is in a state which comprises a significant number of holes. Conduction, which has to be through electron current, does not take place to any great extent. As the voltage rises, the channel becomes less strongly enhanced, and at around zero volts it will start to deplete as with a conventional MOSFET. However, as the potential is increased further, the depletion regions will spread from the three sides and meet, as shown in Figure 9. When this state occurs, the potential in the channel becomes uniform to within a very small value of about a few millivolts. This causes the whole channel to be able to conduct rather than just the semiconductor surfaces as in the conventional MOSFET. This is the main effect the present invention allows. Greatly increased current flows can occur in this mode as compared with those of the conventional MOSFET.

A further increase in potential causes the device to increase the current flow (Figure 10), and eventually the channel becomes

strongly inverted. At this point, additional inversion charge will be confined mainly to the interfaces as in the conventional MOSFET. However, the volume inversion effect can be increased by ensuring that the dimensions of the device are kept small, this means in the order of nanometres, and it is demonstrated by the corners of the three-sided device.

Returning to the description of the volume enhancement device, a similar structure could operate as an enhancement device if the channel doping was n-type instead of p-type. The device would deplete for negative voltages but enhance for positive voltages: the state with zero applied voltage on the gate electrode and the exact values of potential for the operating modes depend on the gate material used. In either case, in weak inversion or enhancement, the volume effect can be demonstrated.

A p-channel device could be made and would operate in a complementary manner to that of the n-channel device, with the values for applied voltages being reversed in sign.

Figure 11 shows a further embodiment where the device has four sides which are located in a vertical arrangement and thus it might be termed a vertical VIMOSFET or VVIMOSFET. In this embodiment, a semiconducting substrate body 1 is formed with a vertical column having a shape which in a horizontal cross-sectional view would be square or rectangular with small dimensions and this extends upwards from the body 1. This vertical column constitutes the semiconductor island 4.

The device comprises the semiconductor substrate body 1, which is provided with a source electrode connection 16, and which

is covered with a gate dielectric film forming the gate insulation material 2. The insulation material extends up the sides of the island 4. At an upper end, the island 4 carries an electrode which supports a drain electrode lead 17.

Below the top of the island 4, a square or rectangular collar of gate material 7 is supported on the insulation material 2 which surrounds the column. An electrical lead is attached to the gate material 7 to form a gate electrode connection 18.

This construction thus provides a MOSFET device having four sides which in combination define four corners. The presence of this feature will thus promote the appearance of the volume inversion effect which will spread simultaneously from each corner. The construction can thus be expected to exhibit a strong volume inversion effect and give an enhanced performance when in service.

The stages required for the manufacture of the four-sided device are depicted in Figures 12A to G.

The manufacturing process begins with preparation of a p-type substrate body 1 which is formed in this instance of a silicon starting material. On this body 1, an electrode diffusion layer 19 of an n+ material is formed to act as a source electrode (Figure 12A).

An epitaxial or other silicon growth 21 is next formed (Figure 12B) to create a lightly doped layer which will be suitable for the channel region of the device. This layer is of a suitable thickness to form the required channel length and this dimension may be of the order of one micron.

Next, suitable masking and patterning is used to form a small channel area which processes require very fine patterning

techniques. The silicon may then be etched using an anisotropic etching medium such as a plasma machine. This etches the silicon down to the underlying source region, leaving a narrow columnar silicon film (Figure 12C). This portion of the silicon film constitutes the island 4.

The columnar film is then oxidised to form the gate insulation material 2, although any suitable dielectric formation method could be used, and the required gate material 7 is deposited. The selected gate material 7 which may be of polysilicon is patterned and etched using an anisotropic etching medium (Figure 12D).

Then the space surrounding the column and gate material is filled with an insulation material 22 such as would conventionally be achieved by depositing an oxide. Finally, a series of process steps are carried out to etch back the polysilicon gate material and make contact with the top of the device, probably by depositing further layers of polysilicon and etching to give a construction as shown in Figure 12E.

Contacts to the source electrode can then be made with top-accessed contact patterning and etching techniques (Figure 12F) for isolated devices, or by using a substrate connection for a higher current carrying capability such as in a power device (Figure 12G).

The foregoing description of an embodiment of the invention has been given by way of example only and a number of modifications may be made without departing from the scope of the invention as defined in the appended claims. For instance, the step of doping the semiconductor film material may be carried out before

or after this material has been etched to produce the separate CMOS transistor bodies.

The doping may be such as to give a desired conductivity type such as n-channel, p-channel or possibly of both conductivity types as would need to be used in a CMOS process.

In addition, the semiconductor island may be constructed initially to be of a larger area than that intended to be used in the finished device, the excess island area then being removed, for example by an oxidation process. The construction method of the invention in fact provides three or four sides of the island shape which are located in close proximity to one another to allow the volume inversion process to take place. This arrangement can thus give an enhancement in the drive power increase obtainable over that which has been disclosed in the aforementioned prior publications. Instead of forming the region of gate oxide by growth, an alternative process would be to do this by the deposition of suitable material.

The gate conductor material, instead of being of polysilicon, could be of metal, for example tungsten. The 'source' and' gate' electrical connections of the device could be interchanged, if required.

The foregoing description has disclosed the importance of providing two, three or four 'corners' where the rectilinear sides of the semiconductor island area meet. It will be apparent, however, that when the island is made to be of only a few nanometres or less in width it might not be possible to construct this with straight sides and in addition it might not be possible to see even two 'corners'. For

example, with an island that was sufficiently small in width, this might even appear to have a circular cross-section, whilst still exhibiting a strong volume inversion effect.

It appears necessary to provide one or preferably more than one, peripheral portions of the island having a small radius of curvature which will serve as initiation centres to promote development of the volume inversion process.

CLAIMS:

1. A semiconductor device, comprising a body of semiconductor wafer material supporting an electrical insulation layer, the layer carrying a semiconductor island covered by a dielectric film which in turn supports a first electrode area constituting a gate or control electrode, the island forming source and drain electrode areas, the construction further including a conductive region adjoining each electrode area to support external electrical connections for the device, the material of said gate electrode together with the values for depletion width and doping level in the semiconductor island being selected such that operation in a volume inversion or volume enhancement mode can be obtained when suitable potentials are applied to said electrode areas.

2. A semiconductor device as claimed in Claim 1, in which the said island has a shape which includes two oppositely directed side portions.

3. A semiconductor device as claimed in Claim 2, in which the said island has a shape which includes three side portions.

4. A method of construction of a semiconductor device, the method comprising the steps of providing a body of semiconductor wafer material, creating an electrical insulation layer on said wafer, forming a narrow semiconductor island on said layer, doping said island to form a transistor body, forming a dielectric film on said

body, depositing a gate electrode area on said film, forming source and drain electrode areas, laying down an interlayer dielectric material, making contact openings then depositing metal regions to provide external electrical connections for the resulting device, the material of said gate electrode together with the values for depletion width and doping level in the semiconductor island being selected such that operation in a volume inversion or volume enhancement mode can be obtained when suitable potentials are applied to said electrode areas.

5. A method as claimed in Claim 4, in which the said insulation layer is formed by an oxygen implantation, porous anodisation, recrystallisation, growth of silicon on sapphire (SOS), or vapour deposition process.

6. A method as claimed in Claim 4 or 5, in which the said semiconductor island is formed by a photolithography and anisotropic plasma etching process.

7. A method as claimed in any one of Claims 4 to 6, in which the said interlayer dielectric material is formed by a phosphorosilica glass (PSG) or other glass deposit.

8. A method of constructing a semiconductor device, substantially as hereinbefore described.

9. A semiconductor device, substantially as hereinbefore described with reference to the accompanying drawings.

Published 1990 at The Patent Office. State House. 66 71 High Holborn. London WC1R 4TP. Further copies may be obtained from The Patent Office.